

SM2246EN Flash F/W & ISP Release Information – S0218AS
Introduction

This purpose of this document is to provide release information on the SM2246EN F/W and ISP release information

Fix Coverage

- stands for the “new fix” or “new support” in the category
- stands for the “no-update” in the category

■ Tester FW	■ Controller ISP
<ul style="list-style-type: none"> □ Yield Issue ■ Flash Issue <ul style="list-style-type: none"> □ SLC Flash <ul style="list-style-type: none"> □ Samsung Flash □ Toshiba/Sandisk Flash □ Intel/Micron Flash □ Hynix Flash □ Others ■ MLC Flash <ul style="list-style-type: none"> ■ Samsung Flash ■ Toshiba/Sandisk Flash ■ Intel/Micron Flash ■ Hynix Flash □ Compatibility issue □ Tester Bug Fix ■ AP Bug Fix & New Function ■ Feature Enhance 	<ul style="list-style-type: none"> ■ Yield Issue ■ Flash Issue <ul style="list-style-type: none"> □ SLC Flash <ul style="list-style-type: none"> □ Samsung Flash □ Toshiba/Sandisk Flash □ Intel/Micron Flash □ Hynix Flash □ Others ■ MLC Flash <ul style="list-style-type: none"> ■ Samsung Flash ■ Toshiba/Sandisk Flash ■ Intel/Micron Flash ■ Hynix Flash □ Compatibility issue ■ ISP Bug Fix □ Feature Enhance

ISP Revision History

Version	MP Tool version	ISP version	Note
S0218AS	S0121A	S0218AS	<p>This FW supports Intel/Micron L06B & L05B 3D MLC NAND (featuring SLC caching)</p> <ol style="list-style-type: none"> 1. Update Security API to S0214A. 2. Pass uLink 6.0 protocol tests. 3. Apply a workaround for host issue: Data triggering is interrupted by host power mode command. (default off in previous version) 4. Record temperature of RTBB. 5. Issue Fix: HDMA FIFOs may run out. 6. Issue Fix: WL may not be applied due to continuous GC operation. 7. Issue Fix: FW may hang during SATA error handle. 8. Issue Fix: Dram reset may be invalid during BVA reset. 9. Issue Fix: As SPOR occurs during closing a GC destination block, FW should return this process ASAP. (Flush dram as SPOR is enabled) 10. Issue fix: As a error block is found by scanning block flow (during power on flow), FW should not reset its valid page count. (May cause valid page mismatch and worst case rebuild time)
R0605AS	R0508A	R0605AS	<p>This FW supports Intel/Micron L06B & L05B 3D MLC NAND (featuring SLC caching)</p> <ol style="list-style-type: none"> 1. Update Security FW. 2. Support Micron L05B MLC. 3. Add extended CID for quick SATA settings. 4. Add check sum feature for download micro code. (optional) 5. Apply a workaround for host issue: Data triggering is interrupted by host power mode command. (default off in previous version) 6. Record read count for RTBB. 7. Issue Fix: FW may hang during SATA error handle. 8. Issue Fix: thermal throttle should not be applied as temperature < 0 degree. 9. Issue Fix: a corner case FW may lose the index info.
Q1122BS	Q1227A	Q1122BS	<p>This FW supports Intel/Micron L06B 3D MLC NAND (featuring SLC caching)</p> <ol style="list-style-type: none"> 1. Update Security FW to version Q1017A. 2. Update RDT FW to version Q1101RDT: issue fix in RDT

			<p>hour setting.</p> <ol style="list-style-type: none"> Update BootISP to version Q1102A. Support whole drive SLC mode by DAh/DFh command. Modify clear buffer flag algorithm in SATA error handle flow. Improve early move algorithm, processed in read flow as well. Set Vfr of VDT27 to 2.8V for L06B 3.3V devices. Add a workaround method for a host issue. Data triggering is interrupted by host power mode command.(default: off) Add pretest error code 0x2A: C_Pret_TotalFBlockOver8K and 0x2B: C_Pret_CapacityNotSupport. Issue Fix: FW should retrieve retry table after resuming form DEVSLP. Issue Fix: During SATA error handle sequence, HW BVA reset may stop HDMA data transfer. Issue Fix: Rest data in HW front-end buffer may cause the BVA halt from releasing SATA engine. Issue Fix: Before power on build link flow, system block may be seen as error block. Issue Fix: Modify the calculation for disk size reported to host. (Take TCG reserved sector count/shift count into consideration for both ISP and RDT FW) Issue Fix: HDMA count may overflow during closing part read FIFOs. Issue Fix: ID table word 77 bit 7 should be 0. (No support DevSleep_to_ReducedPwrState) Issue Fix: An error NCQ (double tag or out of range LBa ... etc) came during standby mode, FW should not return D2H in ISR. Issue Fix: As program fail handle is disabled, minimum size of cache buffer(for host data) should be 3.5*size of super page, to prevent dram buffer flag issue Issue Fix: Check HW command queue done before applying set feature sequence to NAND flash. Issue Fix: Prevent a corner case that FW may reset SMART Info: SPOR occurs during swapping WPRO block.
Q0406BS_SNDK1Z	Q0331A	Q0406BS_SN DK1Z	<ol style="list-style-type: none"> Update RDT FW to version Q0413RDT, featuring read retry sequence for error bit count over threshold.

			2. Change erase policy for SanDisk 1Z flash: issue erase command in the mode the target block will be.
Q0406AS_ SNDK1Z	Q0331A	Q0406AS_SN DK1Z	<p>This FW supports Sandisk 1z SLC caching only, I/M L06B SLC caching is not addressed.</p> <ol style="list-style-type: none"> 1. Security FW: version Q0126A. 2. Support SanDisk 1znm (SDTNSGAMA) SLC caching.

Note:

1. F/W and ISP update is recommended.
2. History # is denoted by "Version-Date" .

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